CHASSIS DESCRIPTION

The ATC311 is the replacement for the DTV307 it includes:

- Enhanced features over the DTV307
- Entirely new chassis platform + new DM2
- 16X9 only (40", 52", 61" and 65" sizes)

Key Features of the ATC311

- NTSC and 1H inputs displayed at 2H
- Integrated ATSC receiver (terrestrial only – no DSS)
- Analog on analog Picture-In-Picture capability (GPIP) w/ twin tuners
- Two RF inputs
- 2 sets composite inputs w/ S-video
- 1 set front composite inputs w/ S-video and headphone jack output
- 2 multisync component inputs + composite inputs
- 1 Digital Video Interface (DVI) input
- IEEE 1394 “Firewire” interface
- Ethernet connector with integrated Web Browser
- SD Video output from HD source
- 60 watts total audio (15W X2 front speakers, 30W integrated subwoofer).
- Center channel input
- 8 sensor autoconvergence
- Gemstar EPG
- All models with integrated frame comb

ATC311 Power Supply System

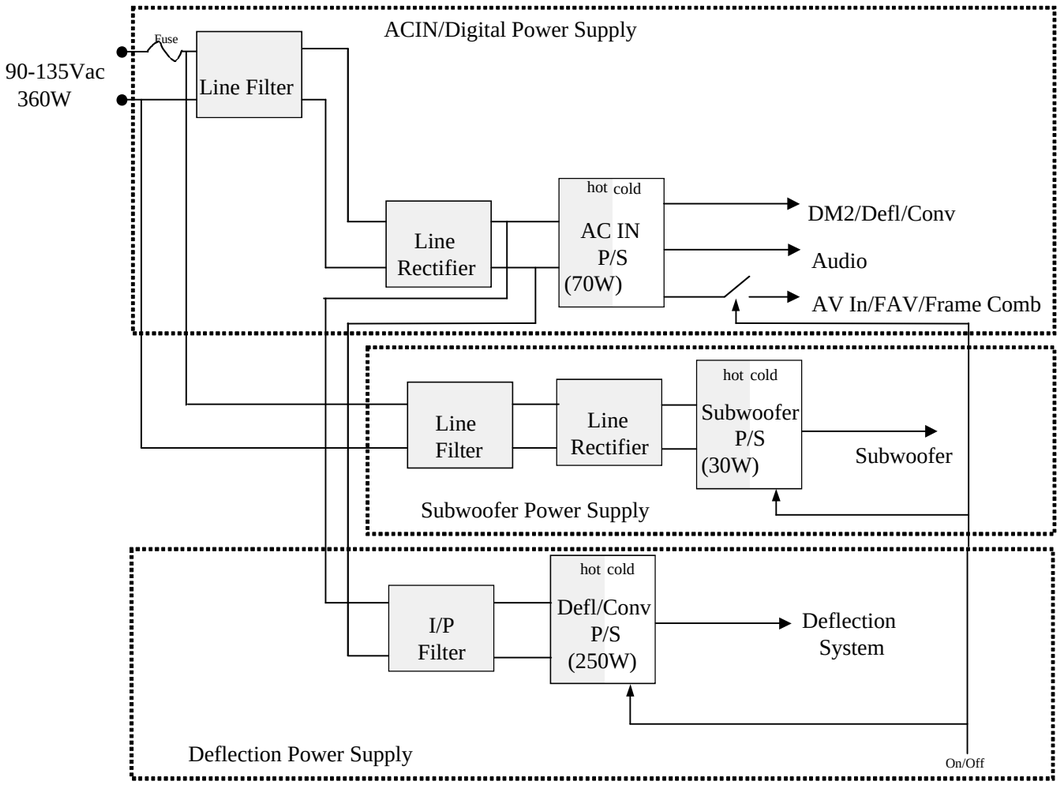
The ATC311 has three distinct power supplies.

1. The ACIN Digital supply used to provide power for the DM2 module, Audio and Frame Comb.
2. Deflection Power Supply which provides power for all the deflection circuitry
3. The Subwoofer Power Supply.

The ACIN Digital supply powers the DM2 module and provides standby power for the chassis. In addition it provides run supplies for audio which are switched using the 15VR run supply from the deflection supply.

The subwoofer supply is on the subwoofer pcb and supplies the voltages needed by the subwoofer output circuitry. The supply takes the filtered AC input from the ACIN Digital supply.

ATC311 Power Supply System



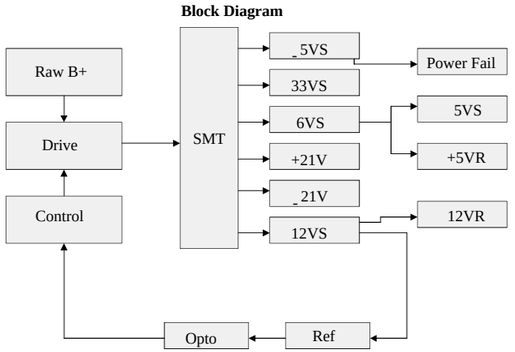
The deflection supply provides the majority of the run supplies which are switched On/Off by the I²C data bus from the DM2 module.

ACIN/Digital Power Supply

Functional Description

The ACIN /Digital power supply used for the ATC311 is a flyback-type, current-mode controlled, zero voltage switching (ZVS) topology utilizing a discrete control circuit and cold-side regulation. The circuit is functionally similar to those used for DVD, MMDS2, and other digital box applications.

Block Diagram



A three-terminal error amplifier IC senses the 12 volt supply and provides feedback to the control circuit through an optoisolator. A power-fail signal is provided to the DM2 module to provide advance warning of an imminent supply voltage dropout.

Circuit Operation

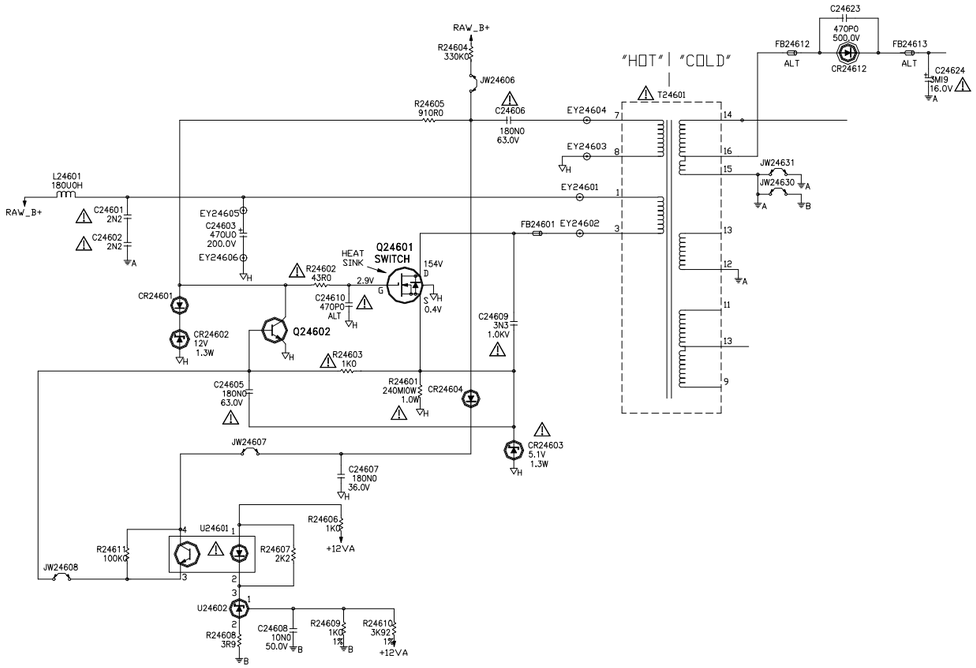
The principle of this power supply is a flyback type zero voltage switching (ZVS) converter operating in the discontinuous mode.

A start-up resistor , R24604, provides the initial gate bias voltage for the MOSFET, Q24601, which begins to conduct. A positive feed back winding (8-7) on the transformer T24601 begins to increase the gate voltage and causes Q24601 to eventually saturate and begin the first cycle of operation. As the current in Q24601 increases, the voltage drop across the current sense resistor, R24601 increases until a threshold level is reached. At this point the transistor Q24602 turns on and the gate drive of the MOSFET is removed. The current flowing in Q24601 drops quickly to zero and the energy stored in the primary inductance of the transformer is transferred to the resonating capacitor, C24609, causing the voltage across the capacitor to rise.

The rising voltage appears across the secondary windings (15-16) and causes a rectifier diode, CR24612, to conduct when the voltage exceeds the voltage across the filter capacitor , C24624.

When CR24612 conducts the energy stored in the primary inductance of the transformer is delivered to the output

ACIN/Digital Power Supply



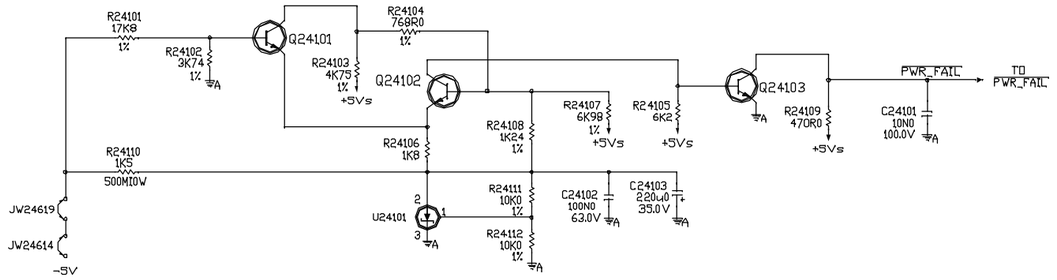
capacitor and the load. When CR24612 stops conducting, the energy remaining in C24609 resonates with the transformer primary inductance, driving the drain voltage of Q24601 towards zero. When the drive voltage tries to go below zero the internal drain to source diode clamps the voltage near ground. The voltage of the drive winding again goes positive causing Q24601 to turn on and begins the next cycle.

Regulation of the supply is accomplished by monitoring the 12VA voltage output. AC line isolation is provided by the optoisolator U24601. As the output voltage increases, the amount of current flowing in error amplifier U24602 increases. This causes an increase in the current through the optoisolator U24601. This causes the voltage at the base of Q24602 to increase which adjusts the point at which the transistor turns on by varying the bias voltage at the base. The increasing voltage reduces the current trip threshold and the current in the MOSFET is decreased. This lowers the energy stored during each cycle and maintains a regulated output voltage.

Additional Design Features

- Switched Run Supplies 12VR & 5VR :
  The 15VR supply from the Deflection Power Supply turns on the 12VR and 5VR supplies
- Power Fail Signal:
  The unregulated negative supply for the –5V follows the raw B+. Q24101 and Q24102 are normally on and Q24103 is normally off. Thus the collector of Q24103 is high. When raw B+ goes below a threshold, Q24102 turns off and the collector of Q24102 goes high. This turns on Q24103 and thus the collector of Q24103 goes low and issues a PWR_FAIL signal.

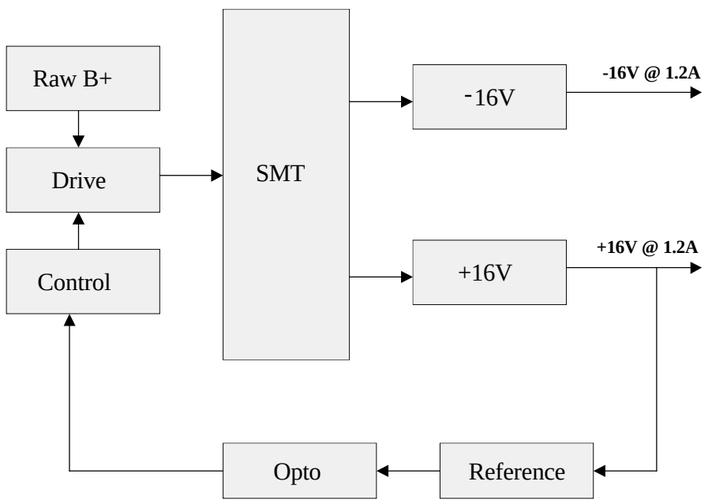
Power Fail Circuit



Subwoofer Power Supply

The power supply used for the subwoofer is a flyback-type, current-mode controlled, zero voltage switching (ZVS) topology the same as the ACIN Power Supply. It utilizes a discrete control circuit for turn on/off controlled by the DM2 system control software and cold side regulation. A three terminal error amplifier IC senses the 16 volt supply and provides feedback to the control circuit through an optoisolator software in the DM2.

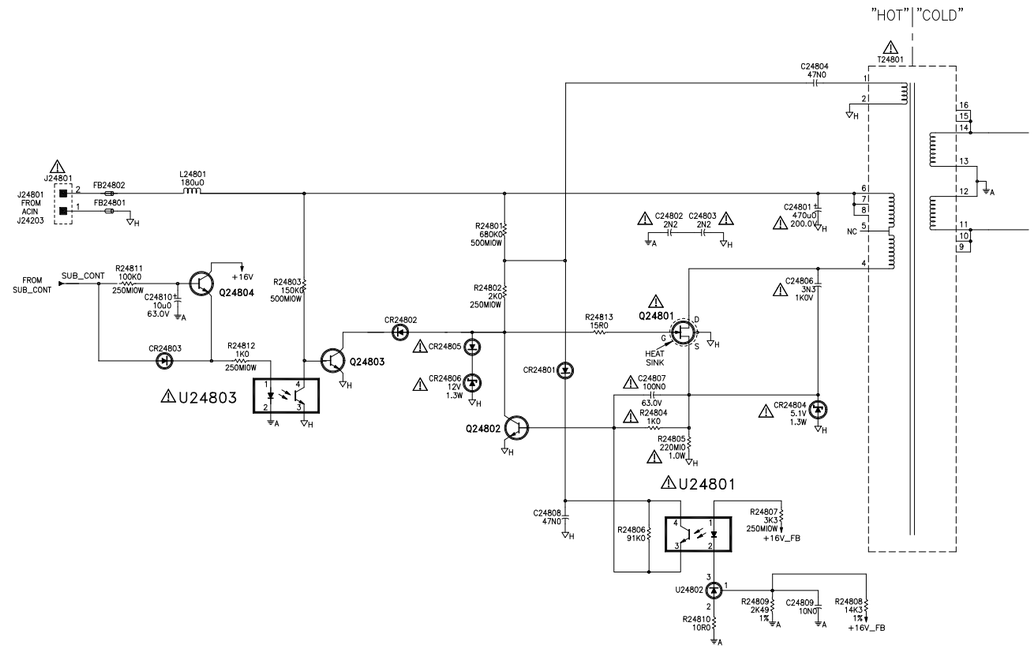
Subwoofer Power Supply Block Diagram



Circuit Operation

Basic circuit operation is the same as the ACIN Digital Power Supply discussed in the precious section. Normally the gate of the MOSFET, Q24801 is pulled low and there are no output voltages. A “ON” signal is applied from the SUB_CONT line to the optoisolator U24803, which turns off Q24803. The SUB_CONT line comes from the Bus Expander, U11501, on the Audio PCB which is controlled by the I²C bus from the DM2. The gate of Q24801 is pulled high through R24801 and R24802 to the Raw B+ and turns on the supply.

An error amplifier U24802 monitors the +16V_FB output voltage and adjusts the point at which the transistor turns on by varying the bias voltage at the base of Q24802. AC line isolation is provided by the optoisolator U24801. As the output voltage increases, the amount of current flowing in U24801 increases which causes the voltage at the base of Q24802 to increase. The increasing voltage reduces the current trip threshold and the current in the MOSFET is decreased, which lowers the energy stored at each cycle and maintains a regulated output voltage.



Deflection - Scan Power Supply

Overview

The main run power supply used for the ATC311 is a flyback-type, current-mode controlled that utilizes a discrete control circuit and cold-side regulation. A three-terminal error amplifier IC senses the scan supply and provides feedback to the control circuit through an optoisolator.

The scan supply B+ must be able to be switched between two different voltages to make the correct raster width at both 2H and 2.14H horizontal frequency. It must do this at the same time as maintaining the correct voltages for all other supplies taken from this SMT circuitry.

Control lines to the scan supply come from the Deflection_DAC, U14850, and include SMT_ON_OFF, REGB+_SW and B+_ALIGN. The DAC is controlled through the I²C data bus from the DM2 module. SMT_ON_OFF is used to turn the scan supply On/Off and the B+ voltage level is controlled by the REGB+_SW and B+_ALIGN control lines.

Different taps on the SMT transformer are used to provide +31 Volts, +15 Volts, +20 Volts and a –20 Volt supply in addition to the scan supply. The tap supplies are further used to derive +24 Volts, +12 Volts and a +45 Volts.

A regulated +9 Volt run supply is generated by taking power from the +12 Volt standby supply and two regulated 12 Volt supplies are generated with discrete regulators on the +24 Volt and +12 Volt supplies.

The high voltage is monitored in case the voltage becomes excessive which could cause X-rays. In this case an X-ray protection circuit will shut the main supply down using the XRP_LATCH control line.

A line from the control DAC, B+_Align, is used to adjust the scan B+ voltage so that the raster width can be controlled.

The SMT_ON_OFF line from the control DAC is used to turn the Scan Power Supply On/Off. A separate TA1316_ON_OFF line is also used to turn the +9VR supply On/Off since the timing is different for the +9VR supply versus the Scan Power Supply

Operation

Raw_B+ voltage is supplied from the ACIN board through connector J14101 whenever AC power is supplied to the instrument.

The supply is turned On/Off with control circuitry lines to the optoisolator U14150. When the set is in standby or in XRP Latch no current flows through Q14150 or the LED of U14150. The base of Q14151 is pulled to RAW_B+ through R14152 making the base forward biased. Q14151 pulls the base of Q14102 low forward biasing the transistor and causing current to flow. This pulls the Gate of MOSFET Q14101 low turning the scan supply off.

To turn on the scan supply the SMT_ON_OFF line goes high at the base of Q14150 causing current to flow through it and the LED in U14150. This in turn reverse biases the base of Q14151 turning the transistor off. This causes the base of Q14102 to rise turning it off . This causes the gate voltage of Q14101 to rise which turns on the MOSFET . When Q14101 begins to conduct the field on the primary of T14101 collapses inducing current into the secondary windings of T14101. As current increases in Q14101 the voltage across the current sense resistor R14109 increases until the base of Q14103 is forward biased. Once turned on Q14103 pulls down the base of Q14102 which turns the transistor on. This removes the bias voltage on the gate of Q14101 turning it off.

Current flowing through Q14102 and R14113 latches Q14103 off. Q14103 remains latched until the voltage across R14113 falls to a point where Q14103 turns off. R14113 is also connected to the output of the optoisolator, U14101, used to regulate the scan supply. If the voltage on the optoisolator

ATC311
CIRCUIT OVERVIEW

side of R14113 is varied then the bias point on the base of Q14103 is raised or lowered. Varying the bias point on Q14103 will vary the on time of Q14101 varying the current transferred to the secondary of T14101. The secondary REG_B+_FBA supply is monitored by U14103 which increases or decreases the current flowing through the optoisolator U14101 based on the REG_B+_FBA loading. This provides the isolated feedback path with which to regulate the scan supply.

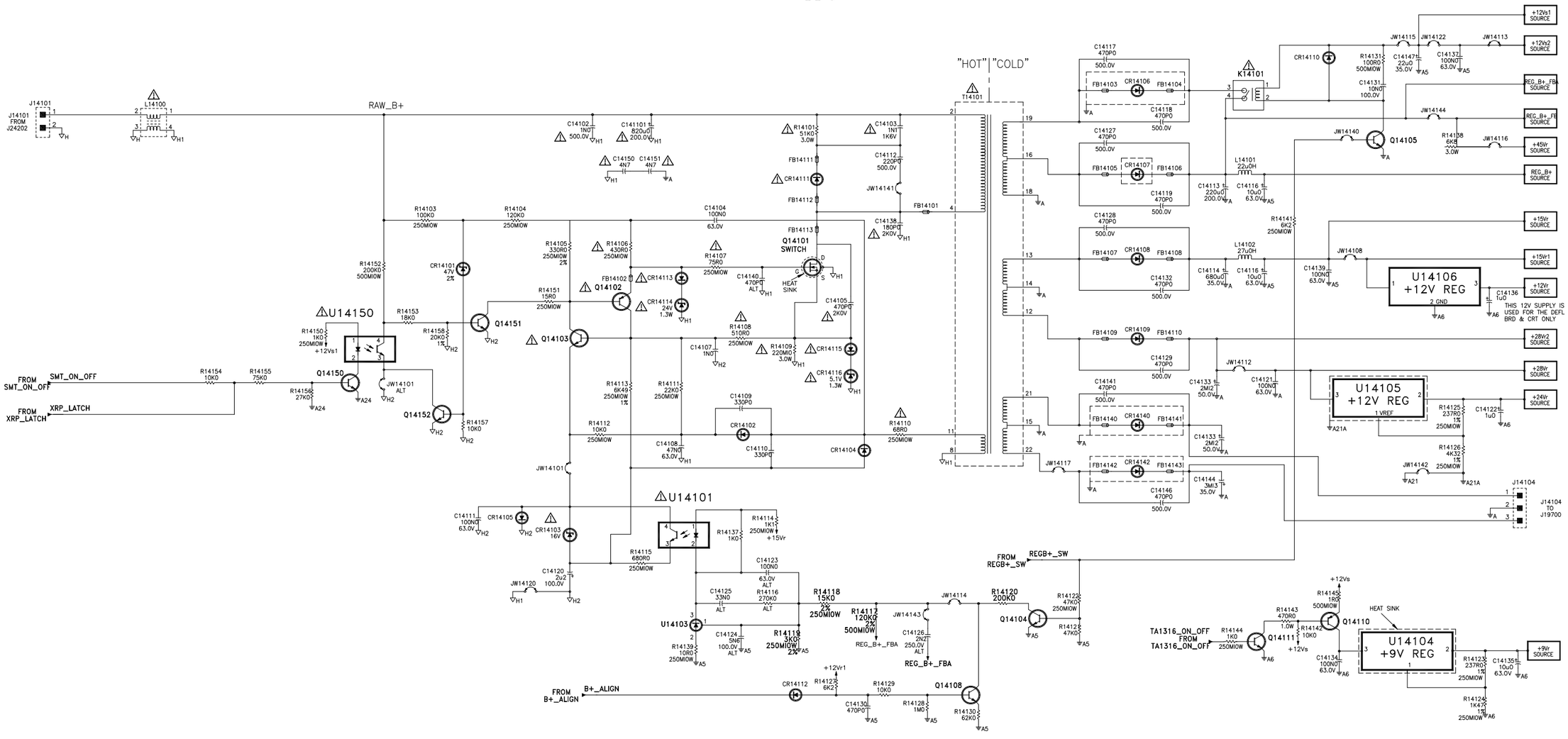
The control line REGB+_SW is used to change the level of the RegB+ for either 2.0 or 2.14H. RegB+ is increased for 2.14H when the control line REGB+_SW is taken high. One branch of this line turns on Q14105 which provides ground for the relay, K14101, this provides additional REGB+ through the tap off pin 19 of T14101 and diode CR14106. This control line also goes to Q14104 in the feedback circuit.

With Q14104 turned on R14120 is placed in parallel with the resistor network of R14117, R14118 and R14119. This lowers the level of the sampled voltage fed to U14101.

The fine adjustment of the scan B+ voltage is accomplished by varying the DAC voltage applied to B+_ALIGN line to Q14108 which in turn controls the feedback reference voltage. This base voltage is adjusted in the factory and stored in memory for proper scan width at both 2.0 and 2.14H.

The +9Vr supply is controlled by the control line TA1316_ON_OFF. This control line comes directly from the DM2 module via J14801. When the control is taken high the base of Q14111 is forward biased and lowers the base voltage of Q14110 which turns on. With Q14110 on the +12Vs is supplied to the 9 volt regulator U14104 which produces +9Vr for the Deflection Processor, U14802, and associated circuitry.

Scan Supply



Deflection

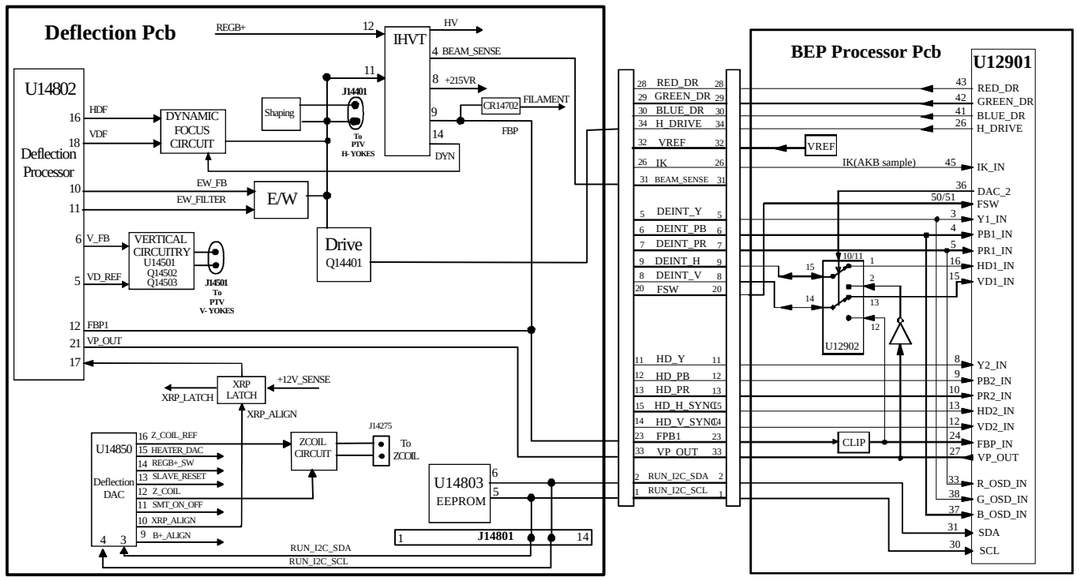
The ATC311 deflection system consists of two levels, Low Level Horizontal and Vertical Processing and the Yoke Drive Output circuitry.

The low level deflection processing is performed using a chip set on both the Back End Processor (BEP) pcb and the deflection pcb which are mated and aligned in the factory.

The BEP is populated with the U12901 Backend Processor (BEP) and the switching IC, U12902. The horizontal PLL and H/V countdown circuits are contained in U12901, while the switching IC, U12902, is used to select the source of the deflection timing signals.

The vertical ramp generator, the East West parabola generator, and the dynamic focus waveform generators are contained in U14802 on the deflection board. The deflection board also contains a 4k EEPROM, U14803, so that alignment data can be stored locally. There is also an octal DAC, U14850, which is used to minimize the number of hardware connections between the deflection board and the DM2.

The deflection pcb also contains the main run supplies mention previously, the horizontal drive circuit, the horizontal output transistor (HOT), IHVT and vertical yoke drive circuit.



Backend Processor Operation

U12901 located on the BEP is a component signal and sync processor for use in multiple frequency applications. The main source of power for this IC is +9Vr. The +9Vr supply is switchable via the TA1316_ON_OFF control line from the DM2 to allow switching off the BEP module during Standby mode. An I^2C bus interface is used for adjustment and alignments.

Input signals to the deflection system have a horizontal frequency of either 2H or 2.14H and can be from either the DM2 or an external source from the AVIN pcb.

The DM2 deflection signal lines to the BEP are labeled DEINT_H and DEINT_V and are connected to U12902 switching IC at pins 14 &15. The external signals coming from the AVIN board are labeled HD_H_SYNC and HD_V_SYNC and are connected directly to U12901 at pins 13 & 12 respectively. These signals are selected by the system control code depending on which input is used as the source.

The matrix switch, U12902, is used to switch timing signals depending on the mode of operation. When the video is from the DM2, the switch routes DEINT_H and DEINT_V drive on pins 14 & 15 of U12902 to pins 15 & 16 of U12901. When the sources are 2H or 2.14H external component signals, the switch (pins 2 & 12) is used to route the VP_OUT timing signal from U12901through U12902 to the DM2 along with the FBP signal from the IHVT on the deflection board. These timing signals are sent to the DM2 to synchronize the OSD system to the external video signal.

The output of the HPLL is the H_OUT signal, which is used to drive the horizontal driver circuit on the deflection board. The duty cycle of the H_OUT waveform can be adjusted by I^2C bus.

A vertical timing pulse is supplied from U12901 to synchronize the various vertical rate timing generators in U14802 deflection processor. This pulse is generated by the vertical countdown circuit. Vertical frequency characteristics are controlled by I^2C bus.

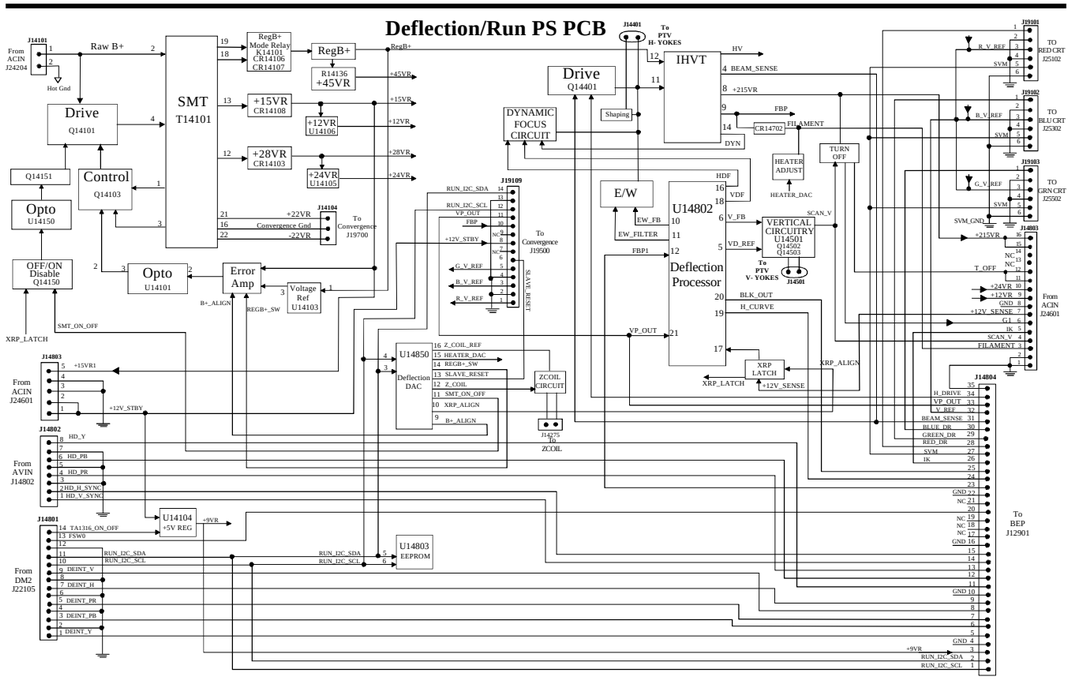
Horizontal and vertical blanking signals are also generated in U12901. An external input is available for use with an analog blanking signal generated by U12901.

U14802 - Deflection Processor Operation

U14802 is the deflection processor IC, which incorporates EW pin correction, vertical ramp generation and distortion correction, and dynamic focus correction, circuits. The various IC functions are adjustable via the I^2C bus. The same +9 volt regulator used by U12901 also supplies this IC.

U14802 requires two timing inputs to synchronize to system vertical and horizontal timing. A vertical rate timing pulse is received from U12901 as mentioned before. A FBP pulse from the horizontal output circuit is used to supply Horizontal timing. The vertical input pulse leading edge is used to generate an internal vertical pulse using the TC filter at pin 22. This pulse is used to generate a vertical rate ramp by utilizing the Vramp filter at pin 23. This common ramp is used to generate all of the vertical rate waveforms generated by the vertical, EW, and DF circuits. For the ATC311 application, the FBP input is only used to drive the HDF section of the IC.

U14802 has an EHT input which allows beam current information to be supplied to both the vertical and EW pin correction circuits. This input can be used to compensate for raster size change due to less than ideal high voltage regulation. The IC has separate I^2C bus adjustments of the gain of the compensation circuits for vertical and EW so that the performance can be independently optimized.



Horizontal Deflection

The horizontal output circuit generates the high current ramp waveform used to drive the horizontal yokes. It also drives the flyback transformer, which in turn produces the supplies necessary for picture tube operation. The supplies include the High Voltage, the focus supply, the screen supply, cathode B+, and the heater voltage.

The horizontal yoke current is provided by a circuit consisting of a switch (HOT and damper diode combination), the primary inductance of the IHVT, a retrace capacitor, the trace capacitor (S-Shaping capacitor), and the horizontal yoke coils.

The voltage supplies provided by the horizontal deflection system are derived from secondary and tertiary windings on the IHVT. These supplies are provided for the video amplifier, the CRT, and the horizontal driver.

The low level signal processing circuits for the horizontal deflection system are contained in U12901 and include the horizontal sync processor.

X-Ray Protection Circuit

High Voltage shutdown is accomplished by sensing a secondary IHVT pulse, rectifying it, and if the sensed signal exceeds safe limits, driving the SMT_ON_OFF line low. Reporting to the microcomputer is accomplished by reading the “X-Ray Protection bit” of the U14802 IC. The microcomputer will then turn off the power supplies, turn the power supplies back on, and attempt to restart the instrument.

The X-Ray Protection (XRP) latch is an open-collector output that removes the Regulated B+ Power Supply by pulling the control line XRP_LATCH low if a fault is detected. Also an X-Ray Fault is reported to the Control System over the

I²C bus when IC, U14802, reports a “Power Supply Disturbance” on pin 17. The first occurrence of the XRP is interpreted as a fault condition, and the microprocessor will attempt to restart the Main Power Supply after 1.5 seconds by toggling the Main Power On control. The x-ray protection circuit is aligned to set the latch before the anode voltage can rise to a level where it can induce CRT radiation exceeding acceptable limits. This circuit produces a DC voltage that is proportional to the CRT anode voltage. This voltage is compared to a discrete voltage reference.

East- West pincushion correction and width adjustment are driven by a linear pincushion driver. The parabola used to develop the correction waveform is generated in IC, U14802. U14802 provides bus control of the horizontal width and pin amplitude as well as horizontal trap correction and corner correction. In addition, a voltage developed across the high voltage return resistor is summed at the pin driver to compensate for the decrease in width that occurs as the high voltage increases with decreasing beam current.

Vertical Deflection

The vertical deflection processing is done in two parts. First IC, U12901, includes the sync separator and countdown circuit, that provides the negative going vertical rate pulse, VP_OUT to IC, U14802. This pulse is also used to synchronize the digital convergence. Second, U12901 also develops the vertical blanking signal, which starts with the vertical pulse and ends at a programmable line count. An additional programmable blanking signal is provided for use in the compressed vertical deflection mode that starts before the vertical sync pulse.

IC U14802 receives the VP_OUT pulse at its pin 21 and develops the vertical deflection ramp, at pin 6, V_FB . The IC also provides a dc reference at pin 5, VD_REF, which tracks at twice the ramp center value. These two signals after a source resistor and restive divider respectively become V_RAMP and V_REF respectively, and are coupled differentially to the vertical output IC, U14501, which drives the yoke. Vertical kill is achieved by I²C bus control of U14802.

U14802 develops the vertical ramp using a ramp capacitor at pin 23, VRAMP_FILTER. If this capacitor has significant changes in series resistance during aging, the ramp amplitude and DC value can be adversely affected. A timer involving the components at T filter, pin 22, sets the reference ramp clamp time. If this time constant were too long, it could cause flat scan at the top of the picture.

Digital Convergence

Overview

The Digital Convergence Integrated Circuit (DCIC) and amplifier system generates 6 convergence yoke drive currents that correct the geometry of the 3 colored pictures from the projection tubes such that they are rectilinear and convergent on the PTV screen. For horizontal and vertical directions in each of the three colors, values for a matrix of 13 vertical points by 16 horizontal points (1248 total) are stored in nonvolatile digital memory. This information is converted by digital to analog converters into 6 analog signals that are power amplified to supply the drive for the convergence yokes. In the vertical direction the signals for scan lines that are between the lines with adjustment points are calculated by the DCIC using smoothed interpolation. In the horizontal direction the DCIC output is digital steps that are smoothed internally by digital filtering and externally by analog low pass filtering. The data values for both convergence and focus are adjustable via I²C bus commands. Each data point can be individually changed (dynamic adjustment) or the entire raster of a color may be moved (static adjustment). The effects of the Earth’s magnetic field change with the placement of the TV and cause picture distortion and misconvergence. These distortions are automatically corrected using a micro processor and data from optical sensors located around the edge of the screen. The customer can then optimize the red and blue center convergence to green. A video test pattern is generated by digital convergence to aid in the customer and service adjustments. Convergence adjustment is required for each mode, 2H and 2.14H, for the initial factory setup, when a major component is replaced or when the receiver is moved to a different magnetic field. In the factory a vision system and external computer are used to initially determine the convergence data values. In field service a PC can be used with Chipper Check Software to speed the alignment process.

Automatic Alignment

A menu item starts the autoconvergence function. If a sensor fails to work, auto alignment will be aborted. Light sensors are placed around the edges of the picture. These sensors sense lighted target edges in each of the three colors. Convergence parameters are then changed by the micro computer to adjust the picture size, shape and position to compensate for picture movement due to magnetic fields, electrical drift or mechanical drift. This system should locate the target edges of all 3 colors within +/- 1mm of the sensor center.

At the start of auto alignment, the screen will blank and color blocks will appear on screen in the screen section for each of the eight (8) sensors in sequence. Brightness is calibrated for each color and sensor display then the values are stored in memory. Next a block shaped pattern will be displayed in the area for each sensor at each color. These lighted areas will be moved by the static convergence adjustment in a preset search pattern until an edge location is detected. An edge is calculated by detecting the edge position from opposite directions on the edge and averaging the two detected locations

A memory record is kept of the required horizontal or vertical movement at each sensor. In the factory, after convergence alignment, a similar process is used to locate the sensors and record their positions. The values of the current sensor locations can then be used to calculate the difference between the current values and the factory recorded values. The picture can then be repositioned and resized to restore proper geometry and convergence. Since there is no center sensor, the average of the screen edge sensor locations is used to shift the center. A small center convergence error may be

introduced by this process. To optimize the center convergence, the customer can fine adjust the match of red and blue to green at the picture center using the convergence menu. To correct the errors introduced by moving the red or blue centering, the micro processor will then recalculate the convergence grid for the entire picture using the new center values.

Operation

The ATC311 convergence system has essentially the same operation and circuitry as the MMC102 and DTV307. Differences are listed below:

- New Board Configuration with combined amplifier and generator board with double sided copper
- Simplified power amplifier circuit
- Simplified opto-sensor detector circuit
- Convergence power is from chassis “run” switch mode power supply and Disconnect Switch to protect circuit components

The new board configuration combines the convergence generator and power amplifier functions in a small compact package. Four cables connect to the board for: power, signals, yokes and opto-sensors. A fifth plug connects to DCAS for alignment. The double sided design eliminates extra bottom side shielding, jumpers and all bottom side chip parts.

Power Amplifier

The power amplifier is similar to the MMC102 circuit. A dual transistor is used at the amplifier input to improve temperature drift performance. The power transistors are the same as used in PTK195 instruments. The amplifier requires only +/-20V supplies so low voltage drive transistors can be used. Signal mute switching is incorporated into the amplifier eliminating it from the generator circuit.

The convergence amplifier compares the voltage applied to the input to the voltage across the sense resistors and supplies whatever yoke current is required to make these voltages equal. At TV turn on the amplifiers are muted because the input signals will be inappropriate until after the convergence IC is programmed from the EEPROM stored values. The two current source transistors can be turned off with the AMPMUTE control signal.

The circuit uses multiple sense resistors to increase their resistance accuracy and reduce thermal drift. Ferrite beads are used to stop high frequency oscillations of the power transistors. A bias transistor is used in the vertical amplifiers to reduce the transients due to cross over of the power amplifier when the input signal switches polarity. The horizontal amplifiers do not use the bias transistor or emitter resistors. The vertical power stage emitter resistors prevent shoot through currents. The crossover picture distortion is not visible for horizontal direction convergence corrections.

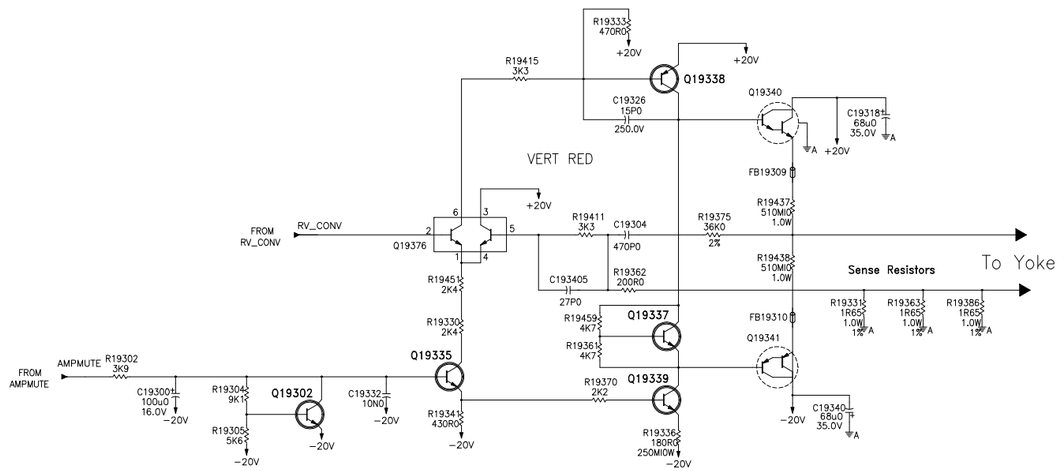
Opto-sensor Detector

The detector sensitivity circuits used in previous product have been replaced with color detecting switches. These lower detector sensitivity for red and blue. This eliminates sensitivity setup time from the auto converge sequence. The AC coupling has been simplified and a one shot pulse circuit has been added to eliminate short light detection pulses that might be ignored.

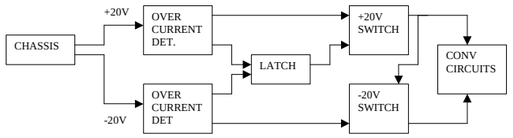
Convergence Power and Disconnect Switch

In previous products the convergence has had its own separate power supply that turned off if a fault existed. For the ATC311, convergence power comes from the chassis run supply. If the run supply is turned off, trouble shooting is very difficult. Convergence fault protection comes from two transistor switches that open and latch when the normal power

Convergence Power Amp



supply current is exceeded in either the +20V or –20V convergence supply.



Over current is detected by comparing the voltage drop across a current sensing resistor against a fraction of a 20V supply. A differential transistor circuit is used to compensate for temperature. The latch is a NPN/PNP feedback pair. Once the latch is on, chassis power must be turned off to reset it. The +20V switched output controls the –20V switch so that +20V comes on first and turns off last. A filter circuit is used in the over current detectors so that a fault must exist for several milliseconds to trigger the latch. This allows high currents at start up to charge the filter capacitors in the convergence circuits. Very high currents that might damage the switch transistors are prevented by drive limiting zener diodes that limit drive voltage to the switch transistors.

Video

The ATC311 has three areas where video signals are input. The external inputs on the Front A/V board (FAV), external aux inputs on the AVIN board and through the RF inputs and DTV Link on the DM2 module. The signals from the FAV board are routed through the AVIN board so this discussion can be limited to just the DM2 module and the AVIN board.

DM2

The DM2 module has 2 RF inputs labeled ANTENNA A INPUT and ANTENNA B INPUT. Antenna A is a Tuner/IF module that contains a tuner section and dual IF section. The tuner is capable of processing both digital and analog RF signals (ATSC/NTSC) from either terrestrial or cable sources. The tuner is a single conversion, electronically aligned tuner with improved cross-modulation, UHF image rejection, and local oscillator phase noise performance over the DTV307 tuner. Performance is tailored to handle the predicted signal environment during transition to digital terrestrial television (HDTV) service, 256QAM digital cable, as well as providing “cable ready” NTSC performance as specified by the FCC. Antenna B is the PIP tuner and is NTSC only.

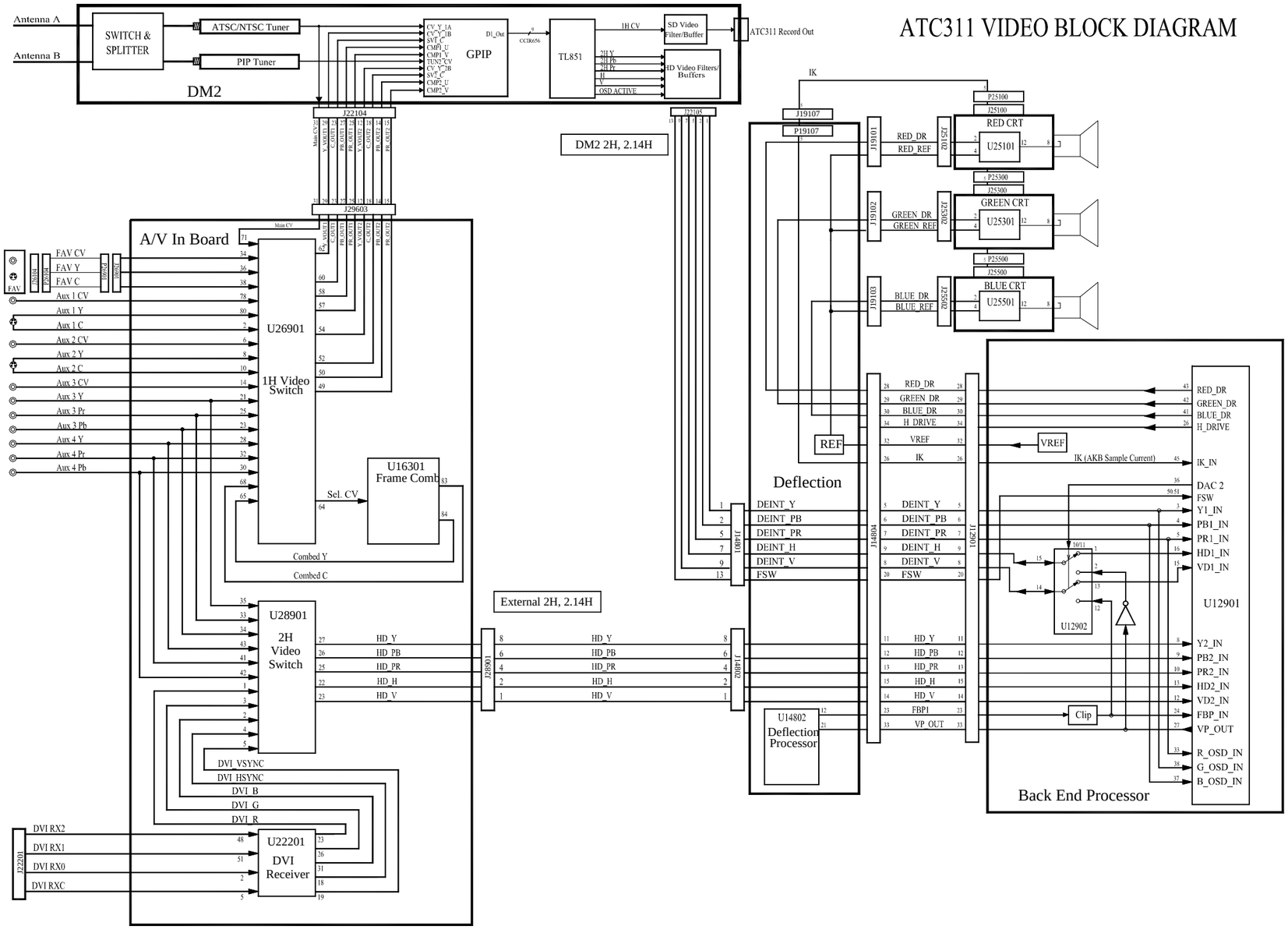
The DM2 has 2 DTVLink connectors which are a compressed digital video inputs offering an IEEE-1394 type video connection for consumer devices such as satellite receivers, cable receivers, and digital recorders that meet the CEA specifications for DTV Link. DTV Link is better known as 1394 or FireWire for digital televisions. Audio and video information is carried on a single wire.

The DM2 module in the ATC311 contains a GPIP IC that performs NTSC decoding of component, SVHS, and composite video signals. It also does chroma decoding of composite and Y+C signals, and adaptive combing of composite signals. The PIP function in the ATC311 is performed by the GPIP IC. It has two video channels. The secondary channel

is scaled down in size and inserted into the main channel to provide the picture-in-picture functionality. GPIP includes a data slicer able to recover teletext, closed caption or Gemstar data signals that accompany input video. All 1H video inputs including signals from the AVIN board are digitized on the DM2 in the GPIP IC for direct input to the video capture port (VSC) on IC, TL851. The output of the IC is digitized YCbCr data compatible with ITU-R BT.601. The GPIP IC produces a horizontal sync signal which is used in the DM2 to generate a line-locked clock. This is the means of maintaining frame-lock between the input and output of the DM2 The GPIP digital output goes directly to the IC, TL851.

TL851 is an MPEG-2 video decoder, display processor with scan rate converter, and graphics accelerator. For 1H video inputs, the output will be up-converted to 480p and the display will be locked to the incoming video. The TL851 recovers HDTV video signals in Y, Pb, Pr format from received bit streams and processes them for display. The HD output will be YPrPb, either 1920x1080i, for HD inputs (1080i, 1080p, or 720p) or 1920x480p for SD inputs. An integrated graphics accelerator renders text and graphics to an independent on-screen display (OSD) bitmap.

The TL851 has 3 outputs, Analog SD video (CVBS), Analog HD video (YPrPb) and Audio Out. The HD video output provided to the chassis consists of Y, Pr, Pb, H and V outputs and an OSD active indicator. The D/A converters output the analog Y, Pb and Pr signals into identical 100-



ohm delay-equalized low-pass filters. The output of the filters is applied to a triple operational amplifier with 75 ohm source terminations that provides the HDTV output. The amplifier is designed to drive 75 ohm loads. Video outputs have no accompanying sync.

For all MPEG and NTSC sources the H & V syncs are driven by the TL851 through a pair of buffers to the chassis. A dual buffer with tri-state output and sync enable control is used for the sync outputs, this allows the same signal paths to be used to provide sync back into the DM2 from the deflection pcb when the video source is a 2.0 or 2.14H signal through the AVIN board. This allows the DM2 to provide sync timing for the OSD.

The DM2 also provides a composite Video Record Output. Output voltages are developed by the encoder DACs drive three identical 75 ohm low-pass filters. Outputs from the filters are applied to a triple op-amp that provides CVBS output source terminated with 75 ohms.

AVIN

The AVIN board located above the DM2 module is populated with external input jacks that accept Composite Video (CV), S-Video, component video (YPrPb) and digital video in its native format (DVI). The sources of input video on the AVIN board can be either NTSC/1H or HD/2H/2.14H.

The Front A/V (FAV) panel has one component video input as well as a S-Video connector which is routed to the AVIN board via cable.

The AVIN board has both CV and S-Video connectors available for both the Aux1 and Aux2 inputs.

The AVIN board has 2 sets of component video inputs (YPrPb), Aux3 and Aux4.

The AVIN board also has a DVI connector. DVI-HDTV is an uncompressed, digital video interface designed to deliver digital video in its native format. It supports the overlay of high-resolution graphics used by some program guides and interactive devices. The DVI receiver IC U22201 decodes the DVI video bitstream. The output is RGB H/V, which goes to U28901 for switching and matrix conversion to YPrPb. The DVI receiver also has a static signal that indicates when a DVI stream is detected. This line is connected to IC U26901's GPIO1, so that it can be read via the bus.

Source selection for NTSC/1H sources (stereo audio, composite, S-Video, and component) is provided by IC U26901 for rear input jacks, FAV jacks, as well as for the main tuner video (Main_CV) from the DM2. A frame comb filter is provided to optimally comb any composite source into an S-Video (Y/C) output source which is routed back into U26901. All composite and luma inputs to U26901 have sync detectors that are readable via the I²C bus which allows for automatic source selection.

As mentioned above a frame comb filter is provided to optimally comb any composite source in U26901 into an S-Video (Y/C) output source. The frame comb circuitry, U16301, incorporates the typical external 4Mbit of DRAM onto the same die as the frame comb itself. This IC is designed to perform comb filtering of the composite signal by comparing and processing sequential frames as opposed to the standard line combing method.

Source selection for HD/2H/2.14H sources (component and DVI) are provided for rear inputs (2 component and 1 DVI) with the IC U28901. This IC is a 4-input video switch with signal format detection, a matrix circuit, gain switchable outputs, and I²C control.

- Video presence detectors are available on all composite and S-Video inputs. These are used for autodetecting S-Video and YPrPb source. Note: these ***will*** detect the presence of 2H Y sources also for Aux3 and Aux4 Inputs.
- Sync presence of the YPrPb inputs are detected in U26901. Then, U28901 selects that input, so that the horizontal frequency of the sync on Y can be found. If the horizontal sync is found to be 1H then the signal will be fed through U26901 to the GPIP IC in the DM2. If the horizontal sync is 2H or 2.14H, then the signal will be fed directly to the deflection pcb then through to the BEP.

For 2.0 and 2.14H YPrPb inputs, the chassis separates horizontal sync from the luma with composite sync. This horizontal sync signal is then routed to the DM2. From this sync signal the DM2 generates a line-locked clock of roughly 27MHz. This signal along with horizontal and vertical sync supplied from the chassis are routed to the TL851 IC in the DM2. The TL851 uses the sync signals provided by the chassis to reset its timing generators, and create an OSD pixel clock with a PLL locked to the incoming line-locked clock.

Video Processing

The video processing in the ATC311 is broken into several sections: chroma processing, deinterlacing processing, luminance processing, color difference processing, external YPrPb processing, OSD RGB processing and RGB output processing. The chroma decoding is performed in the DM2 module in the GPIP IC.

Luminance Processing

Except for the deinterlacing, the luminance processing is done in the back end processor (BEP) IC, U12901 . U12901 has two component video input ports. Luminance from the DM2 (DEINT_Y) at either 2H or 2.14H is applied to Y1_IN through a clamping capacitor. External 2H or 2.14H YPrPb luminance (HD_Y) from the AVIN board is applied to Y2_IN through a clamping capacitor. Following the Y1/Y2 inputs in U12901 is a luminance switch that selects the input source. The switch is I²C bus controlled. Following switching, the luminance signal undergoes the following processing in the IC:

- Black Stretch
- Black Level Correction
- Dynamic Gamma Processing

- Controlled DC Restoration
- Sharpness Control
- Edge Replacement
- High Frequency White Peak Limiting
- Sub Contrast
- UniColor (Ganged Contrast and Color Level)
- Clamping
- White Peak Limiting
- Output Gamma Processing
- Half Tone Processing

Beam limiting is done in the clamping and UniColor stage. After half tone processing, the luminance is applied to the RGB matrix.

Color Difference Processing

The chroma decoding is done in the GPIP IC in the DM2. The output of the GPIP IC is a digital CCIR 601 stream and is fed to the TL851 IC. The TL851 provides 2.0 H and 2.14H color difference signals from the DM2 to the Backend Processor. The signals are Pr (DEINT_Pr) and Pb (DEINT_Pb): the signal amplitudes are 0.7V peak to peak on a 100% color bar signal.

External 2H or 2.14H YPrPb color difference signals are fed from the AVIN module (HD_Pr, HD_Pb), to the Back End Processor via cable to the deflection board.

The Internal Pr and Pb signals are capacitively coupled to Pr1_IN and Pb1_IN inputs, and the external Pr and Pb signals are capacitively coupled to Pr2_IN and Pb2_IN inputs. The color difference inputs are clamped during the horizontal blanking interval. From the PrPb inputs the signals are routed through switches that are ganged to the luminance switch. After the switch the signals go into a switchable matrix that converts the input signals to YUV format. The matrix will convert signals matrixed according to either SMPTE 170M or SMPTE 274M (NTSC/SDTV or HDTV) to standard color difference levels. This allows the system to process the color difference signals properly regardless of standard.

Following the matrix conversion, the YUV signals are converted to YIQ for use in the Auto Flesh circuit. Auto Flesh can be disabled, and is bus controlled. After the Auto Flesh stage, the I and Q signals are converted back to U and V.

Following the I/Q to U/V conversion the signals undergo the following processing:

- Tint Control
- Color Edge Correction
- Color Control
- UniColor (Ganged Contrast and Color Level)
- R-Y Rematrix (Bus Programmable)
- G-Y Matrix (Bus Programmable)
- R-Y Color Gamma
- Half Tone
- Blue Enhancement
- Clamping

After clamping, the R-Y, G-Y and B-Y signals are applied to the RGB Matrix with the luminance to generate RGB signals. Beam limiting is done in the UniColor stage, just as it is for luminance. This means that the RGB signals are controlled by beam limiting, but by means of controlling the luminance and color difference separately.

OSD RGB Processing

Whenever an external 2H or 2.14H signal (including DVI) is selected, the OSD can no longer be part of the video as it is with internal signals which pass through the DM2 module. The OSD is an RGB signal from the DM2. The OSD RGB and a fast switch signals are applied to the BEP U12901 from the DM2. The OSD signals are carried from the DM2 to the Backend Processor on the YPrPb lines. The fast switch line controls the correct timing of OSD to video. There are two fast switch inputs on the Backend Processor; however, since there is only one fast switch line from the DM2, the two FSW inputs are tied together on the BEP board. When the OSD inputs to the Backend Processor are above 0.7 volts, the SVM output signal is disabled. The OSD signals are coupled into the IC via clamp capacitors. After clamping, the signals are amplified and applied to a switchable OSD beam limiter. The OSD beam limiting is separate from the video beam limiting. After beam limiting, the OSD signal is mixed with the video RGB in the ratios determined by the levels of the two fast switch signals.

U12901 also has an analog RGB input, but it is a simple input with only a brightness control. There is no contrast control and no beam limiting.

RGB Output Processing

The RGB signals from the OSD/Video RGB matrix are applied to variable gain stages, two of which are controlled by the I²C bus. The ATC311 controls the gains of the Red and Blue channels, leaving the Green channel at fixed gain. The gains of the amplifiers are adjusted to achieve the desired display color temperature. The values of the Red and Blue amplifier gain are modified to change color temperature from Normal to Warm or Cool. To set the color temperature for Warm, the Red gain is increased and the Blue gain is reduced. To set the color temperature for Cool, the Red gain is reduced and the Blue gain is increased.

After the RGB signals are gain controlled, they are applied to a set of clamps. These clamps are used to set the output DC levels of the RGB signals. The clamps are controlled in one of two ways. It is possible to set the clamp level, and thus the DC level, via the bus. This mode is used at initial turn on to ensure that the AKB system does not drive the cathode-grid diode to forward bias. The normal mode of operation of the ATC311 is with AKB on. A time-multiplexed pulse is applied to each color at the end of vertical retrace. These pulses generate beam currents in the three CRT guns. The currents are "clamped" in a fashion similar to the MM101 and DTV307, except that there is a current clamp on each kine socket board. These clamps are neces-

sary to remove unbalanced currents from the outputs of the kine driver IC's. After the current clamps, the currents are summed and fed back to U12901. At U12901, the currents are converted to voltages, clamped and compared to internal reference voltages. The AKB system adjusts the DC levels of the RGB outputs until the pulse voltages at pin 45 of U12901 that are generated from the beam currents match the internal references. The references are adjustable via the bus, and can be used to adjust low light color temperature. Adjusting the reference values changes the peak value of the AKB pulses at pin 45. The AKB system maintains the black level of the signal at the cathodes due to the feedback.

After the clamps, the video signals have horizontal and vertical blanking applied to them. The blanked signal is applied to output buffers and is output on the RGB pins of the IC.

Because of the length of cable from the Back End Processor to the CRT board, an NPN transistor buffers the output of U12901. To maintain temperature stability of the DC operating point, an additional PNP emitter follower is used. The blanking of the RGB signals is limited in its downward excursion. This is done to keep the Kine Driver IC's out of deep cutoff so that they come from horizontal blanking without excess time delay. A divider on the emitter of the NPN emitter follower adjusts the minimum blanking level.

CRT

The ATC311 product uses an IC for the kine drivers. AKB & Beam Limiting is provided by the Back End Processor (U12901). A current reference for AKB is DC coupled from each IC driver. Grid Kick and Scan Loss are provided to protect CRT devices.

Audio

The ATC311 audio system hardware resides on three assemblies.

The "AVIN" module which contains the A/V switch IC U26901 and all the baseband input jacks.

The DM2 module performs demodulation of the audio from off-air sources (NTSC and HDTV). It contains the tuners and IF demodulators, ATSC decoding IC's, and a mixed-signal audio processing IC.

The Audio module performs most of the baseband audio processing – volume control, graphic equalizer, subwoofer support, and power amplification with speaker switching. It also contains the SRS feature processing and an I²C bus expander.

AVIN

The AVIN board located above the DM2 module is populated with external input jacks for the various Video and Left/Right Audio Inputs jacks. The L/R inputs include audio from Aux1, Aux2, Aux3, Aux4 and DVI.

The Front A/V (FAV) panel has one set of L/R audio jacks which are routed to the AVIN board via cable.

Source selection for external stereo audio is provided by the switch IC U26901 for rear input and FAV jacks. The signal output of U26901 is routed to the DM2 module.

DM2

The DM2 audio system performs the following functions:

1. Decodes audio from NTSC sources. Outputs are Left and Right stereo, or SAP.
2. Decodes the Dolby Digital audio stream from ATSC sources. Outputs are mixed-down Left-total and Right-total.
3. Input Left and Right signals from baseband sources (output of the A/V Switch on the AVIN board) and digitize them for processing.
4. Perform audio processing – delay (for lip-sync) and level compression – on the active source as needed.

The ATSC/NTSC tuner and its associated IF and demodulator circuit provides the off-air signal from which the audio is taken. The second PIP tuner provides video only for PIP. The ATSC/NTSC tuner has two simultaneous outputs. One output is a 4.5MHz sound subcarrier, which passes through a bandpass filter and a buffer-amplifier prior to delivery to the Multistandard Sound Processor IC U11603. This is the path for NTSC audio. U11603 demodulates stereo and SAP then makes it available at the routing switch.

The second output of the tuner is the recovered ATSC mode digital bitstream. This signal is ATSC 8VSB at near-baseband. The TL851 IC parses the audio and decodes Dolby Digital, performs delay for video lip-sync if needed, then provides a Dolby Virtual Surround 2-channel (Lt and Rt) mixdown in I²S form to IC, U11603, where it is available at the routing switch for processing.

I²S *(Inter-IC Sound) is a serial bus design for digital audio devices and technologies such as digital sound processors, and digital TV (DTV) sound. The I²S design handles audio data separately from clock signals. An I2S bus design consists of three serial bus lines: a line with two time-division multiplexing data channels, a word select line, and a clock line.*

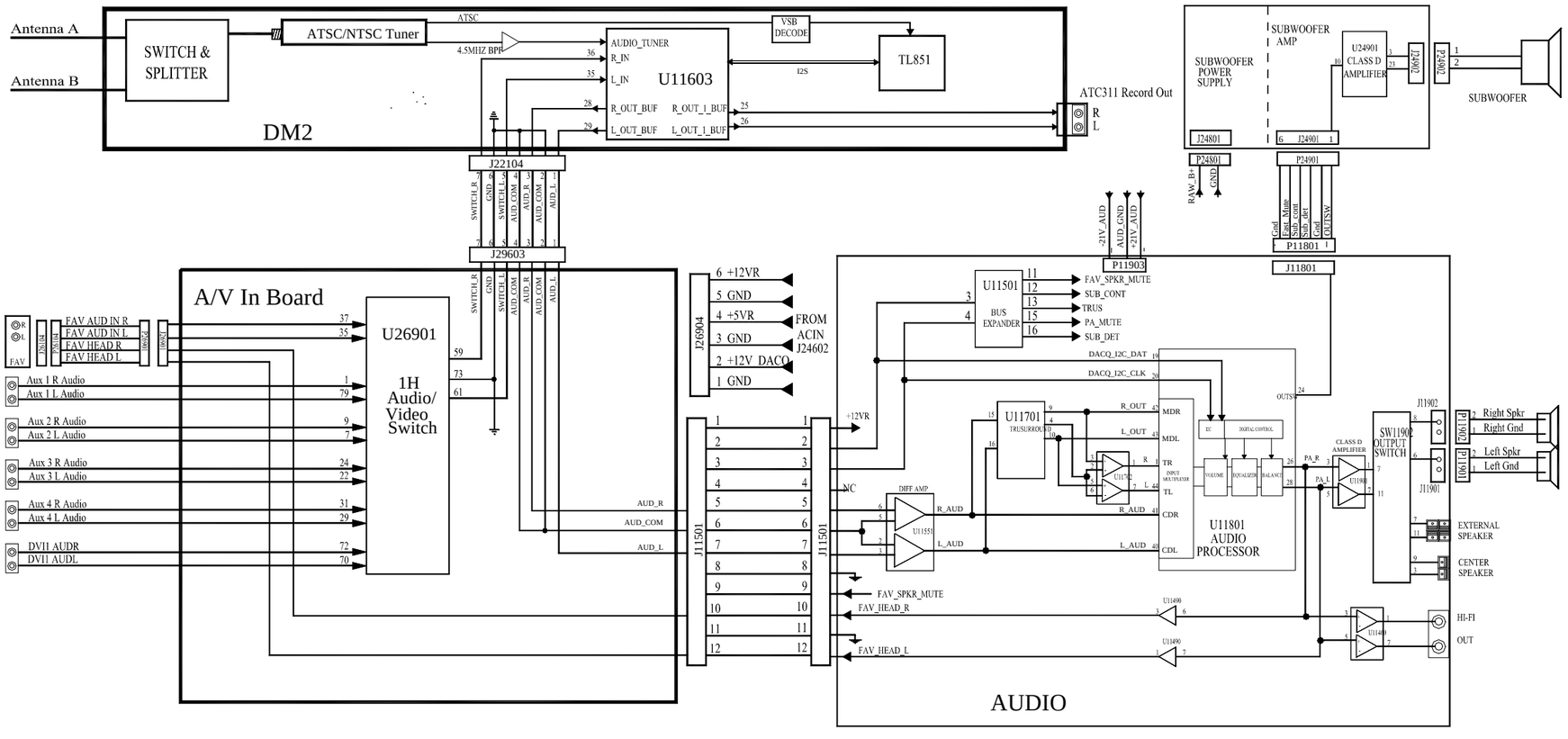
The Left and Right baseband audio from the Aux input jacks is made available at one of U11603 SCART inputs. In either of the analog modes (NTSC or baseband inputs), the needed signal (stereo/SAP or digitized SCART) are digitized and routed to the I²S output and sent to the TL851. The signal is formatted and sent through the lip-sync delay. The delayed signal is converted back to I²S form and returned to the U11603 routing switch.

The U11603 routing switch selects the necessary signal. The audio is converted back to analog and sent to a pair of analog outputs. One path goes directly to the "Record" outputs located on the DM2 module. The other path passes through the Automatic Volume Control block, which performs the "Sound Logic" feature, then is sent to the 31 pin connector at line level. This is routed to the Audio module for processing.

Audio Board

The analog audio from the DM2 is routed back to the AVIN board where it is cabled to the Audio board. There it is input to a differential amplifier, U11551. This amp is used to eliminate ground loops caused by the long cable routing. The output of U11551 is fed to the input of the SRS/FOCUS processing blocks, U11701 & U11702, and directly to one input of the audio processor, U11801. The processor selects one

ATC311 AUDIO BLOCK DIAGRAM



of three inputs, the direct signal (no SRS) from U11551, Regular SRS or TRUSURROUND from U11701 or SRS/FOCUS from a combination of U11701 and U11702.

SRS

The analog input for the SRS circuit is taken off the output of the diff-amp, U11551. The signal is "flat" (unprocessed) and at a constant line-level. The SRS circuitry has two functional blocks in series. These produce two signals which are sent to inputs on the audio processing IC, U11801, along with the direct signal. The two signals are the midpoint of the SRS blocks and the end of the SRS blocks. The processor IC selects which input signal is required for the customer-selected mode. The circuitry operates on +12V power.

The first block, composed of IC U11701 and its support components, performs either Regular SRS or "TRUSURROUND". A control line from the bus expander, U11501, is used to select the mode. The second block , composed of IC U11702 and its support components, performs "Focus", using the op-amp-based circuit provided by SRS Labs.

- Regular SRS mode is selected by using the midpoint of the output of the SRS block and placing it in Regular mode. (Focus is always on but its output isn't selected.)
- SRS Focus mode is composed of Regular SRS plus Focus. The SRS block is placed in Regular mode and the Focus output is also selected.
- TRUSURROUND mode is selected by placing the SRS block in TRUSURROUND mode and using its output.

The input modes are independently selected from each other. The circuit can thus perform all functions built into one version and allow the SRS control line and processor input selector to control the selected mode.

To prevent input ports of the audio processor from being overdriven the SRS IC U11701 is designed with less than unity gain. The software will boost the Volume when SRS is enabled to compensate. The exact boost amounts vary by mode, but are generally about +4dB.

Audio Processor

The audio processor has three input signals applied to the selector, direct audio from U11551, SRS from U11701 and Focus from U11702. After the signal is selected in the processor, volume control is applied. The ATC311 system does not have a separate tone control function but a 7-band graphic equalizer is available. After the equalizer, L and R signals are summed and split off to form two signal paths. The summation stage output signals are run through a highpass filter for the main channels, and a matching lowpass filter for the subwoofer. The subwoofer volume is therefore controlled by the main volume, but a fader is provided in the subwoofer path (accessed by the "Subwoofer Level" menu) so that it's level may be adjusted relative to the main channels. Three analog outputs from the processor provide the Left, Right, and subwoofer signals.

Audio Output

PA_L and PA_R audio signals from the processor are routed to three circuit areas.

- To U11460, which drives the HiFi Output jacks located on the Audio module. The buffer-amp provides approximately 15dB of gain.
- To the main power amplifier, U11901.
- To the headphone amplifier, U11490. The output of U11490 is routed through the AVIN module to the headphone jack which is located on the FAV module.

The subwoofer output from the processor is routed to connector, J11801. The subwoofer amplifier module plugs into this connector. Also present on the connector are two control lines that sense the presence of the subwoofer option and turn the amplifier and power supply off and on.

Power Amplifier

A class-D power amplifier IC, U11901, is utilized for the stereo audio output. The amplifier IC can be placed in standby mode when the set is off or when the speakers are turned off in the menu. The amplifier is controlled through the mode control pin (6). This pin is controlled by a line from the bus expander (PA_MUTE). The majority of ATC311 models are rated for 15+15 watts and in those the amp is operated without limit except for supply voltage and speaker impedance. For lower-power, 5+5 watt, versions the threshold of the AVR (Automatic Volume Reduction) circuit is set for approximately 7 watts. The power amplifier receives its main supply, +/-21 volts, from the ACIN module.

The output-switching scheme varies by model. The base version has the "matrix surround" feature as used in earlier product. Some versions will have a speaker-level center channel input, which allows the set's internal speakers to be driven by an external surround decoder. The switching will put the internal speakers in series and isolate them from the internal amplifier; the input is applied to a two-pin speaker jack. Two mechanical switches are used – one, SW11902, to select INT/EXT SURR or EXT for the main speaker jacks, and the other, SW11901, to enable the center channel input.

Since the amplifier operates in split mode with direct output coupling, it must have the DC Detector function to protect the speakers. This circuit is essentially a lowpass-filter. The output is monitored by a control line to determine if excessive amounts of DC voltage are present. The line goes to the bus expander and is made available to the system micro. If the line goes high the power supply is turned off.

An AVR (automatic volume reduction) circuit is also provided at the outputs. The output of this circuit is monitored by the control line AVR to the bus expander, U11501. When the control line AVR (AC level) exceeds a predetermined threshold, the line to the bus expander goes high and is made available to the system micro. The volume is reduced by software to keep the power below the threshold.

Bus Expander

As mentioned previously the Audio module contains a bus expander, U11501, connected to the system micro via the I²C bus. The bus expander on the Audio Module uses its ports to select the following functions:

- SRS mode
- Volume control
- Graphic Equalizer
- Subwoofer autodetection and mode
- Main power amplifier mode (standby/play)
- Sense of AVR (Automatic Volume Reduction)
- Sense of DC Detection

Subwoofer

The subwoofer system is a plastic enclosure and speaker assembly mounted to the rear panel of projection instruments. A cable connects the speaker to a separate amplifier/power supply module that is mounted to the PTV optronics frame. Another cable conveys control and signal information from the Audio module to the amplifier/PS module. Rectified power line (+160vdc) is cabled from the ACIN assembly to the amplifier/PS module. The amplifier is a stereo class-D IC, U24901, operating in bridge mode to deliver approximately 30 watts.

System Control

The DM2 module in the ATC311 performs the system control, user interface and VBI decoding functions previously located in either a system control microprocessor or Gemstar 4 module. The key interfaces of the DM2 application software are:

- User Interface, through the IR keyboard, IR remote, and FPA
- Inter-Integrated Circuit (I²C) bus communication.
- VBI, for collection of information from the analog interface.

User Interface

The FPGA IC, U23210, in the DM2 module is used for decoding the user interfaces in the ATC311. U23210 is a Programmable-Logic-Device packaged as a 208-pin Plastic-Quad-Flat-Pack (PQFP).

The DM2 IR Receiver supports two protocols: Thomson IR-Remote control and IR PPM5 Protocol specification for remote keyboard. IR serially received data is input to the DM2 on pin 7 of J13603.

The DM2 contains a Functional-Block used to scan and detect the buttons on the Front Panel Assembly (FPA). The FPA on the ATC311 has 8 buttons. There are 4 groups of buttons on the FPA. Each group is composed of 2 buttons connected to one KBS (Keyboard Sense) line. Each of the KBS lines are pulled to +5V through a pull-up resistor in the DM2. One button is connected to the KBD (Keyboard Drive) line (odd) and the other button is connected to ground (even).

The keyboard is scanned every 100 ms. On each scan routine, there is a delay of 40 microseconds to read the pins after setting the KBD line. This is used to compensate for capacitance and inductance on the FPA lines. The system control must scan the 4 KBS sense lines twice in order to read a button press. This is because each sense line is connected to two buttons.

First Scan: The KBD (drive) line is set to high-impedance, making the odd buttons invisible since even if one is pressed it's sense line will remain high. If one of the even buttons is pressed, its corresponding KBS sense line will be driven to ground. Thus an even button press can be detected.

Second Scan: The KBD (drive) line is set to ground. If one of the odd buttons is pressed, its corresponding KBS lines will be driven to ground. Thus if the first scan does not detect a low and the second scan does it can be determined that the odd button was pressed.

I²C bus communication

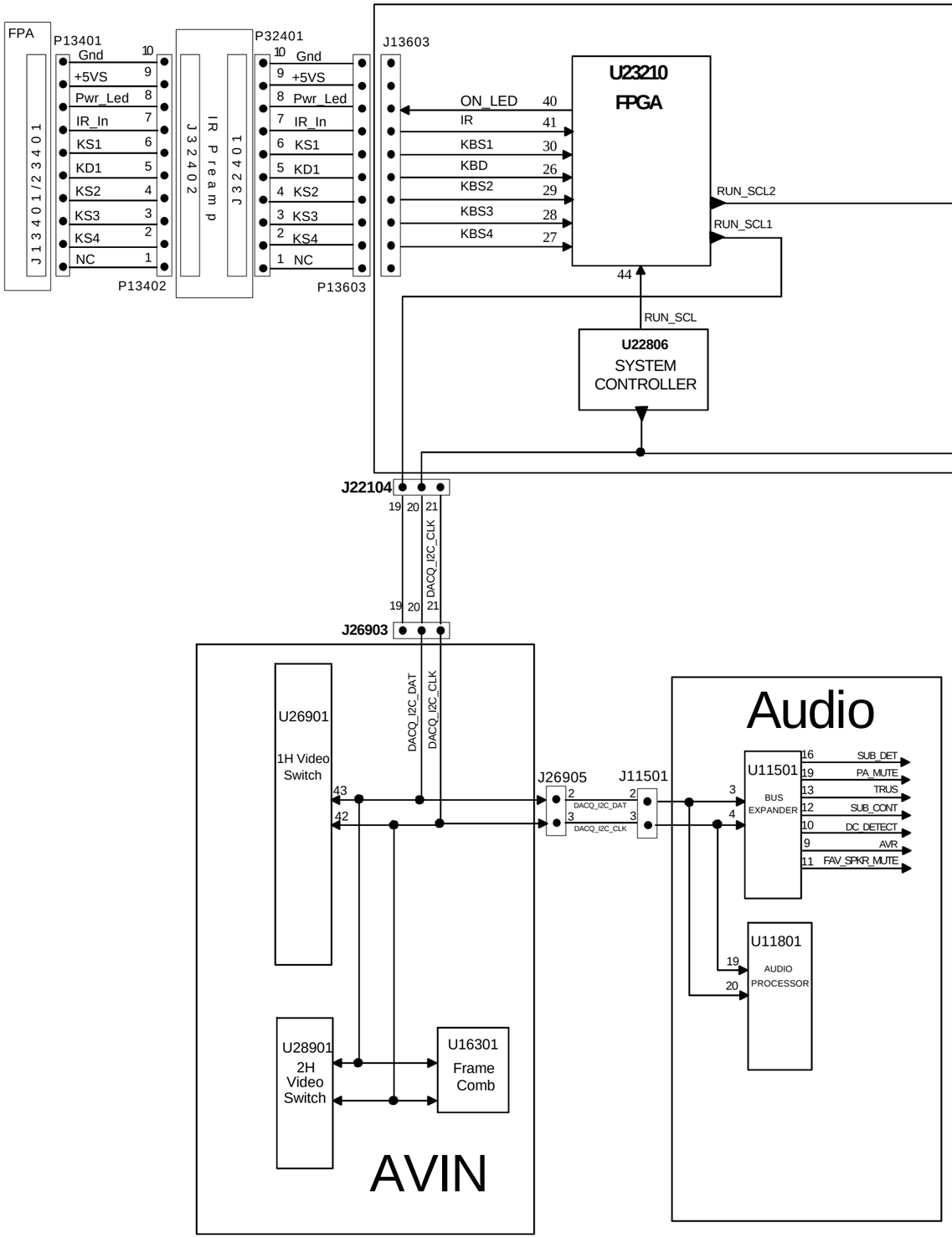
The system controller IC U22806 contains a UART interface that produces the RUN_I²C Bus-Controller that is used to control the ATC311 chassis. The bus is a master/slave interface that tolerates 5 volts.

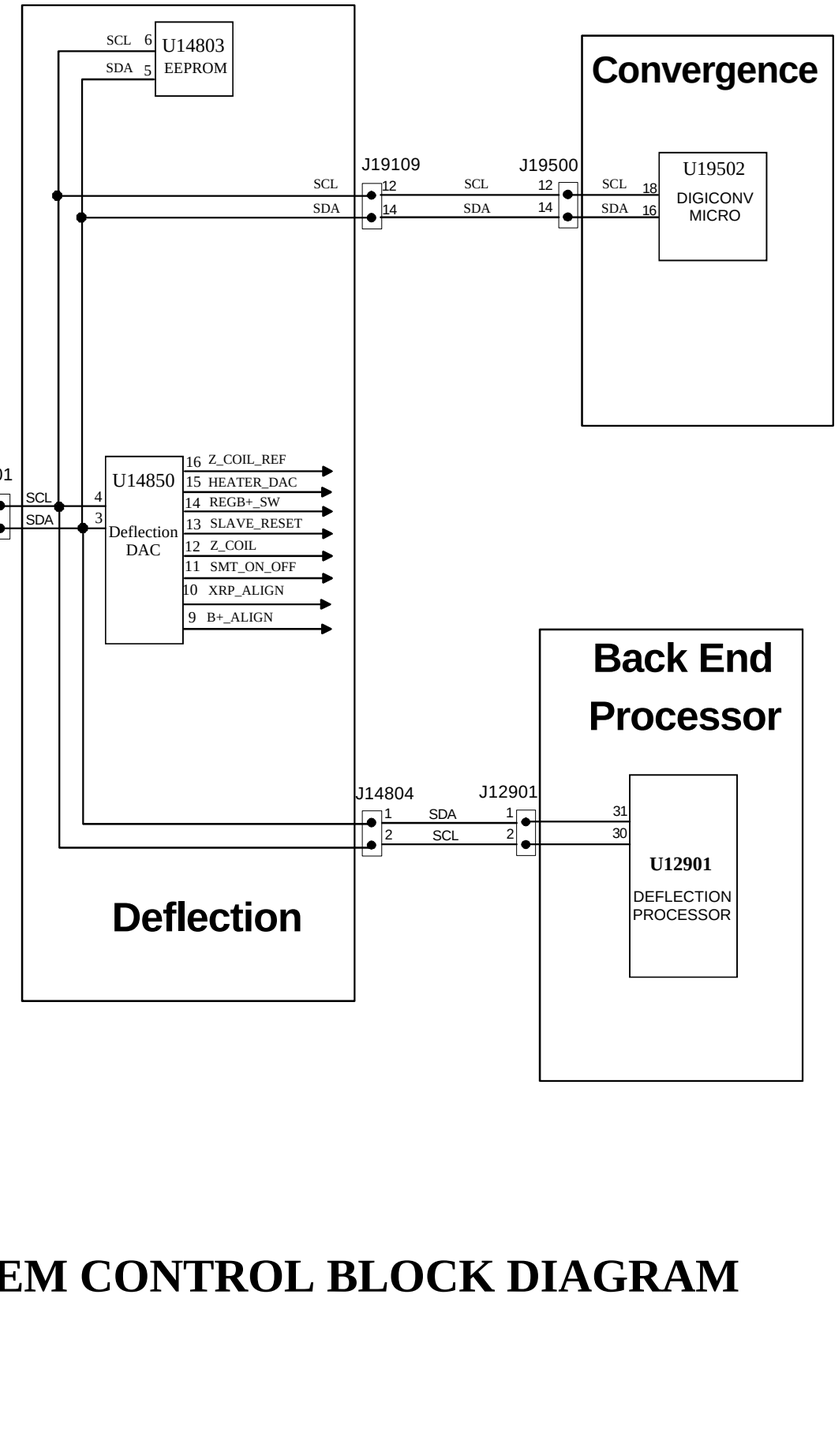
Run Data and Run Clock are generated in the system controller U22806 (RUN_SDA & RUN_SCL). The RUN_SCL clock line is fed to the FPGA IC U23210 where it is divided in the I²C Clock Mux and Stretch circuitry. This switches I²C RUN_SCL to RUN_SCL1 which is used for controlling the Chassis Audio circuitry and RUN_SCL2 which is used in the chassis deflection circuitry.

VBI Data Slicer

The DM2 has two data slicers able to retrieve VBI (Vertical Blanking Interval) information from the video program and send the data over the CCIR656 data stream. The lines to slice are fully programmable over the I²C bus, and the sliced data packets contain a header that indicates what type of sliced data is present. The data slicer is used to recover closed captioning, Gemstar EPG and extended data information.

ATC311
CIRCUIT OVERVIEW





SYSTEM CONTROL BLOCK DIAGRAM